IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): R. Bhattacharya et al.
Case: 1-4-2-2-1
Serial No.: 10/620,045
Filing Date: July 15, 2003
Group: 2123
Examiner: Mary C. Jacob

Title: Method and Apparatus for Automatic Generation of Multiple Integrated Circuit Simulation Configuration

---

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants (hereinafter "Appellants") hereby appeal the final rejection dated November 17, 2006 of claims 1 and 3-19 of the above-identified application.

REAL PARTY IN INTEREST

The present application is assigned of record to Agere Systems Inc. On April 2, 2007, the assignee Agere Systems Inc. completed a merger with LSI Logic Corporation, with the resulting entity being named LSI Corporation. LSI Corporation is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

STATUS OF CLAIMS

The present application was filed on July 15, 2003 with claims 1-19. Claims 1 and 3-19 remain pending and stand rejected. Claims 1, 18 and 19 are the pending independent claims.

Each of claims 1 and 3-19 stands rejected under 35 U.S.C. §103(a). Claims 1 and 3-19 are appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a method of simulating the operation of at least one switch fabric comprising a plurality of integrated circuits using a software-based development tool. The method comprises the steps of providing in the software-based development tool an interface permitting user control of one or more configurable parameters of the switch fabric and automatically generating a simulation configuration for the switch fabric based on current values of the configurable parameters. The simulation configuration is generated without requiring further user input and the simulation configuration specifies interconnections between the integrated circuits which satisfy the current values of the configurable parameters.

In an illustrative embodiment, described in the specification at, for example, page 4, line 4, to page 5, line 28, a method may simulate the operation of at least one switch fabric, which may be, for example, that shown in FIG. 5 or that shown in FIG. 6, comprising a plurality of integrated circuits, such as 106-1...106-N of FIG. 1, using a software-based development tool, such as 100 of FIG. 1. This method includes the step of providing in the software-based development tool an interface (e.g., 104 in FIG. 1 or 200 in FIG. 2) permitting user control of one or more configurable parameters (e.g., 216 in FIG. 2) of the switch fabric. This method also includes automatically generating (e.g., by 115 in FIG. 1 or 308 in FIG. 3), without requiring further user input, a simulation configuration (e.g. 500 in FIG. 5) for the switch fabric based on current values of the configurable parameters, the simulation configuration specifying

interconnections between the integrated circuits which satisfy the current values of the configurable parameters.

Independent claim 18 is directed to an apparatus for simulating the operation of at least one switch fabric comprising a plurality of integrated circuits, the apparatus comprising an information processing device having a processor and a memory. The information processing device implements a software-based development tool providing an interface permitting user control of one or more configurable parameters of the switch fabric, the development tool being operative to automatically generate a simulation configuration for the switch fabric based on current values of the configurable parameters. The simulation configuration is generated without requiring further user input and specifies interconnections between the integrated circuits which satisfy the current values of the configurable parameters. An illustrative embodiment is described in the specification at, for example, page 5, lines 8-10, with reference to the illustrative method heretofore described.

Independent claim 19 is directed to an article of manufacture comprising a storage medium containing one or more software programs for use in simulating the operation of at least one switch fabric comprising a plurality of integrated circuits, utilizing a software-based development tool. The one or more software programs when executed implement the steps of providing in the software-based development tool an interface permitting user control of one or more configurable parameters of the switch fabric and automatically generating a simulation configuration for the switch fabric based on current values of the configurable parameters. The simulation configuration is generated without requiring further user input and the simulation configuration specifies interconnections between the integrated circuits which satisfy the current values of the configurable parameters. An illustrative embodiment is described in the specification at, for example, page 5, lines 8-10, with reference to the illustrative method heretofore described.

The claimed invention provides a number of significant advantages over conventional arrangements. As discussed in the specification at, for example, page 1, line 16, to page 2, line 19; page 3, lines 15-18; and page 5, lines 21-28, illustrative embodiments advantageously allow

for automated determination of an appropriate configuration of integrated circuits within a simulation of a switch fabric, thus reducing the time required for such simulation.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 3, 4 and 6-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Boggio et al., "NetworkDesigner - Artifex - OptSim: A Suite of Integrated Software Tools for Synthesis and Analysis of High Speed Networks," Optical Networks Magazine, Sept/Oct 2001, pages 27-41 (hereinafter "Boggio") in view of Sun et al., "Simulation Studies of Multiplexing and Demultiplexing Performance in ATM Switch Fabrics," Performance Engineering in Telecommunications Network Teletraffic Symposium, 14-16 Apr. 1993, pages 21/1 – 21/5 (hereinafter "Sun").

2. Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Boggio in view of Sun in further view of Ishida et al., "A 10-GHz 8-b Multiplexer/Demultiplexer Chip Set for the SONET STS-192 System," IEEE Journal of Solid-State Circuits, Vol. 26, No. 12, Dec. 1991, pages 1936-1943 (hereinafter "Ishida").

ARGUMENT

1. §103(a) Rejection of Claims 1, 3, 4 and 6-19

Claims 1, 3, 4, 6-8, 11-13, 16-19

The combined teachings of Boggio and Sun not only fail to teach or suggest at least the limitations of providing a user interface permitting user control of one or more configurable parameters of a switch fabric, and automatically generating a simulation configuration for the switch fabric specifying interconnections between the integrated circuits of the switch fabric, but both Boggio and Sun actively teach away from such limitations by instead disclosing arrangements which assume a single fixed switch fabric configuration. See Boggio at page 30, column 1, first paragraph ("In every network design, either manually or automatically generated, all network elements are modeled as having a fixed 'back-plane' with specific connectors.") (emphasis added) and Sun at page 21/3, sixth paragraph ("In this tool only fixed routing mechanism is [sic] implemented. A routing table is used to specify the next queues taken by the

cells to their destinations.") (emphasis added). Thus, Boggio and Sun only disclose conventional techniques for simulation of a fixed configuration which fail to achieve the advantages of the present invention in automated determination of an appropriate configuration of integrated circuits within a simulation of a switch fabric.

Appellants further submit that Sun and Boggio are not analogous prior art and therefore cannot form the basis for a rejection under 35 U.S.C. §103. Even if the Examiner's assertion, found in paragraph 14 of the final Office Action, that Sun and Boggio "are both directed to the modeling of and simulation of a network," were true, it would still be insufficient to establish them as analogous prior art; see, e.g., Wang Lab. v. Toshiba Corp., 993 F.2d 858, 864 (Fed. Cir. 1993) (holding that "art is not in the same field of endeavor as the claimed subject matter merely because it relates to memories.").

Whereas the limitations of claim 1 are directed to generation of an optimal device-level simulation configuration for at least one switch fabric, Boggio is directed toward network-level simulations rather than device-level simulations of such individual network components as switch fabrics. See, e.g., Boggio at page 28, column 1, last paragraph ("This paper specifically focuses on the benefits of combining together three tools to form an integrated suite for the virtual prototyping of optical networks: NetworkDesigner, Artifex, and OptSim.").

Additionally, the Sun reference actively teaches away from the limitations directed to the simulation of at least one switch fabric (e.g., providing an interface permitting user control of one or more configurable parameters of the switch fabric) by indicating at page 21/3, first paragraph, that "[d]imensioning the switch fabric" beyond the "simple configuration" involving a single switch fabric is "beyond the scope" of its disclosure.

With regard to motivation to combine Sun with Boggio, the Examiner provides the following statement in the final Office Action at paragraph 15:

> It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the software development tool for an optical network as disclosed in Boggio et al to include the modeling of a multistage switch fabric . . . . as taught in Sun et al since Sun et al teaches a method for modeling a switch fabric with basic components for simulation to study multiplexing and demultiplexing performance in a network, enabling the switch fabric to be modeled without losing generality.

Appellants respectfully submit that the proffered statement fails to provide sufficient objective motivation for the combination and, rather, is a conclusory statement of the sort rejected by both the Federal Circuit and the U.S. Supreme Court. See KSR v. Teleflex, No. 13-1450, slip op. at 14 (U.S., Apr. 30, 2007), quoting In re Kahn, 441 F. 3d 977, 988 (Fed. Cir. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.").

More specifically, the statement above is using the benefit obtained from a combination as a motivation for that combination and thus constitutes impermissible hindsight. See, e.g., KSR v. Teleflex, slip op. at 17 ("A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning."); Graham v. John Deere Co. of Kansas City, 383 U. S. 1, 36 (1966) (warning against a "temptation to read into the prior art the teachings of the invention in issue").

In order to avoid the improper use of a hindsight-based obviousness analysis, particular findings must be made as to why one skilled in the relevant art, having no knowledge of the claimed invention, would have combined the teachings of Boggio and Sun in the manner claimed (See, e.g., In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000)). The Examiner's conclusory statements do not adequately address the issue of motivation to combine references. "It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to '[use] that which the inventor taught against its teacher.'" In re Sang-Su Lee, 277 F.3d 1338, 1344 (Fed. Cir. 2002) (quoting W.L. Gore v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983)).

Additionally, the statement suggests that would be obvious to modify a software development tool for an optical network to include the modeling of a multistage switch fabric where, as discussed above, these are distinct and non-analogous fields of endeavor.

It is thus believed that the collective teachings of Boggio and Sun fail to meet the limitations of claim 1. Independent claims 18 and 19 contain limitations similar to those of claim 1 are believed to be patentable for similar reasons.

Dependent claims 3-8, 11-13, 16 and 17 are believed allowable for at least the reasons identified above with regard to claim 1.

Claim 9

Dependent claim 9 recites an additional limitation wherein the configurable parameters comprise a configuration type of the switch fabric. In the illustrative embodiment disclosed in the specification with reference to FIGS. 3 and 4 at, for example, page 8, line 12, to page 9, line 2, upon a selection of a configuration type by a user, a switch fabric configuration with that configuration type will be generated by an automated process without additional user input.

In formulating the rejection of claim 9, the Examiner concedes that Boggio does not teach this limitation (see paragraph 12 of the final Office Action); rather, the Examiner contends that it is taught by Sun at page 21/3, paragraph 1 (see paragraph 13 of the final Office Action). Appellants respectfully submit that the combined teachings of Boggio and Sun fail to teach or suggest at least the claimed method comprising steps of providing in the software-based development tool an interface permitting user control of a configuration type of the switch fabric and automatically generating a simulation configuration for the switch fabric based on a current value for the configuration type.

Although the relied-upon portion of Sun discloses that other switch fabric "configurations are also possible such as introducing more switching queues with more complicated routing mechanisms" (Sun, page 21/3, paragraph 1), Sun fails to disclose an interface permitting user control of a configuration type, much less automatically generating a simulation configuration based on a current value of the configuration type. Rather, it explicitly teaches away, stating: "Dimensioning the switch fabric is beyond the scope of this study. This paper concentrated only on the simple configuration illustrated in figure 2." (Sun, page 21/3, paragraph 1)

Accordingly, Sun fails to teach or suggest the limitation wherein the configuration type of the switch fabric is a configurable parameter. Boggio fails to supplement the above-noted fundamental deficiencies of Sun relative to claim 9. Accordingly, claim 9 is believed to be patentable over the proposed combination of references.

Claim 10

Dependent claim 10 recites an additional limitation wherein the interface permits user selection of one of a centralized configuration, a stackable configuration and a distributed configuration for the switch fabric. An illustrative embodiment is described in the specification at, for example, page 7, lines 11-16.

In formulating the rejection of claim 10, the Examiner concedes that Boggio does not teach this limitation (see paragraph 12 of the final Office Action); rather, the Examiner contends that it is taught by Sun at page 21/3, paragraph 1 (see paragraph 13 of the final Office Action). Appellants respectfully submit that the combined teachings of Boggio and Sun fails to teach or suggest at least the claimed limitation wherein the interface permits user selection of one of a centralized configuration, a stackable configuration and a distributed configuration for the switch fabric.

Although the relied-upon portion of Sun discloses that other switch fabric "configurations are also possible such as introducing more switching queues with more complicated routing mechanisms" (Sun, page 21/3, paragraph 1), Sun fails to disclose an interface permitting user selection of a configuration type, much less of a centralized configuration, a stackable configuration and a distributed configuration for the switch fabric. Rather, Sun teaches away by explicitly stating: "Dimensioning the switch fabric is beyond the scope of this study. This paper concentrated only on the simple configuration illustrated in figure 2." (Sun, page 21/3, paragraph 1)

Accordingly, Sun fails to teach or suggest the limitation wherein the interface permits user selection of one of a centralized configuration, a stackable configuration and a distributed configuration for the switch fabric. Boggio fails to supplement the above-noted fundamental deficiencies of Sun relative to claim 10. Accordingly, claim 10 is believed to be patentable over the proposed combination of references.

Claim 14

Dependent claim 14 recites an additional limitation wherein a generation interface declares a generate function that is implemented by each of a plurality of generators, each of

which corresponds to a different configuration of the switch fabric. An exemplary embodiment is shown in FIG. 4 of the drawings and described in the specification at, for example, page 8, line 19, to page 9, line 2.

In formulating the rejection of claim 14, the Examiner concedes that Boggio does not teach this limitation (see paragraph 12 of the final Office Action); rather, the Examiner contends that it is taught by Sun at page 21/3, paragraph 1 (see paragraph 13 of the final Office Action: "(claims 14, 15) the ability to build other configurations (Figure 2, page 21/3, paragraph 1).") Appellants respectfully submit that the combined teachings of Boggio and Sun fails to teach or suggest at least the claimed limitation wherein a generation interface declares a generate function that is implemented by each of a plurality of generators, each of the plurality of generators corresponding to a different configuration of the switch fabric.

Although the relied-upon portion of Sun discloses that other switch fabric "configurations are also possible such as introducing more switching queues with more complicated routing mechanisms" (Sun, page 21/3, paragraph 1), nowhere does Sun teach or suggest an implementation with a plurality of generators, much less one in which each of a plurality of generators corresponds to a different configuration of the switch fabric. Boggio fails to supplement the fundamental deficiencies of Sun relative to claim 14. Accordingly, claim 14 is believed to be patentable over the proposed combination of references.

Claim 15

Dependent claim 15 recites an additional limitation wherein the plurality of generators comprises a centralized configuration generator, a stackable configuration generator and a distributed configuration generator, corresponding to respective centralized, stackable and distributed configurations of the switch fabric. An exemplary embodiment is shown in FIG. 6 of the drawings and described in the specification at, for example, page 8, line 19, to page 9, line 2.

In formulating the rejection of claim 15, the Examiner concedes that Boggio does not teach this limitation (see paragraph 12 of the final Office Action); rather, the Examiner contends that it is taught by Sun at page 21/3, paragraph 1 (see paragraph 13 of the final Office Action: "(claims 14, 15) the ability to build other configurations (Figure 2, page 21/3, paragraph 1).")

Appellants respectfully submit that the combined teachings of Boggio and Sun not only fail to teach or suggest at least the claimed limitation wherein the interface permits user selection of one of a centralized configuration, a stackable configuration and a distributed configuration for the switch fabric.

Although the relied-upon portion of Sun discloses that other switch fabric "configurations are also possible such as introducing more switching queues with more complicated routing mechanisms" (Sun, page 21/3, paragraph 1), Sun does not teach an implementation wherein a plurality of generators comprises a centralized configuration generator, a stackable configuration generator and a distributed configuration generator, corresponding to respective centralized, stackable and distributed configurations of the switch fabric. Indeed, as discussed above with reference to claim 14, Sun fails to teach the claimed plurality of generators and, with reference to claim 10, Sun fails to teach respective centralized, stackable and distributed configurations of the switch fabric. Boggio fails to supplement the fundamental deficiencies of Sun relative to claim 15. Accordingly, claim 15 is believed to be patentable over the proposed combination of references.

2. §103(a) Rejection of Claim 5

Dependent claim 5 recites an additional limitation in which the integrated circuits comprise integrated circuits of a designated chip set utilizable in the switch fabric. In characterizing the Ishida reference as allegedly meeting this additional limitation, the Examiner relies primarily on page 1936, column 1 of Ishida, which the Examiner contends "teaches an ultra high speed 8-b multiplexer and demultiplexer chip set that has been developed for the synchronous optical network (SONET) as a key component of next-generation optical fiber communication systems that will require higher data bit rates for future increases in transmission capacity." (paragraph 24)

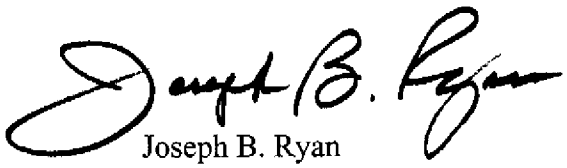
However, within the optical networking context to which Ishida (unlike the present invention) is limited, multiplexers and demultiplexers are distinct components from a switch fabric. See, e.g., Harry G. Perros, Connection-Oriented Networks: SONET/SDH, ATM, MPLS, and Optical Networks 198 (2005) ("An [optical switch] consists of amplifiers,

multiplexers/demultiplexers, a switch fabric, and a CPU."); George N. Rouskas & Lisong Xu, Optical Packet Switching, in Emerging Optical Network Technologies: Architectures, Protocols and Performance 111, 113 (Krishna M. Sivalingam & Suresh Subramaniam, eds.) (2005) ("[A] generic [optical packet switching] node . . . . consists of a set of multiplexers and demultiplexers, an input interface, a space switch fabric with associated optical buffers (i.e. fiber delay lines) and wavelength converters, an output interface, and a switch control unit.").

Accordingly, Ishida fails to teach or suggest the additional limitation of dependent claim 5 wherein the integrated circuits comprise integrated circuits of a designated chip set utilizable in the switch fabric. Instead, it merely teaches integrated circuits of a designated chip set utilizable in a multiplexer and demultiplexer. Thus, the Ishida reference fails to supplement the above-noted fundamental deficiencies of Boggio and Sun relative to claim 5.

In view of the above, Appellants believe that claims 1 and 3-19 are in condition for allowance, and respectfully request the withdrawal of the §103(a) rejections.

Respectfully submitted,



Date: May 21, 2007

Joseph B. Ryan
Attorney for Appellant(s)
Reg. No. 37,922
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-7517

CLAIMS APPENDIX

1. A method of simulating the operation of at least one switch fabric comprising a plurality of integrated circuits, utilizing a software-based development tool, the method comprising the steps of:

providing in the software-based development tool an interface permitting user control of one or more configurable parameters of the switch fabric; and

automatically generating a simulation configuration for the switch fabric based on current values of the configurable parameters;

the simulation configuration being generated without requiring further user input;

the simulation configuration specifying interconnections between the integrated circuits which satisfy the current values of the configurable parameters.

2. (Cancelled)

3. The method of claim 1 wherein the at least one switch fabric comprises at least one multistage switch fabric.

4. The method of claim 3 wherein the integrated circuits comprise at least two ingress devices, at least one cross-connect device and at least two egress devices.

5. The method of claim 1 wherein the integrated circuits comprise integrated circuits of a designated chip set utilizable in the switch fabric.

6. The method of claim 1 wherein the interface includes a listing of the integrated circuits and permits user control of one or more configurable parameters of each of the integrated circuits.

7. The method of claim 1 wherein the interface includes a listing of a base device specified for the plurality of integrated circuits and permits user control of one or more configurable parameters of the base device.

8. The method of claim 1 wherein the configurable parameters comprise a switching capacity of the switch fabric.

9. The method of claim 1 wherein the configurable parameters comprise a configuration type of the switch fabric.

10. The method of claim 9 wherein the interface permits user selection of one of a centralized configuration, a stackable configuration and a distributed configuration for the switch fabric.

11. The method of claim 1 wherein the configurable parameters comprise a number of ports of the switch fabric.

12. The method of claim 1 wherein the software-based development tool comprises an automatic configuration generation module which generates the simulation configuration for the switch fabric based on the current values of the configurable parameters.

13. The method of claim 1 wherein the simulation configuration is generated utilizing an object-oriented programming construct comprising a base class, corresponding to a base device specified for the plurality of integrated circuits, and an associated generation interface.

14. The method of claim 13 wherein the generation interface declares a generate function that is implemented by each of a plurality of generators, each of the plurality of generators corresponding to a different configuration of the switch fabric.

15. The method of claim 14 wherein the plurality of generators comprises a centralized configuration generator, a stackable configuration generator and a distributed configuration generator, corresponding to respective centralized, stackable and distributed configurations of the switch fabric.

16. The method of claim 1 wherein the software-based development tool runs at least in part on an information processing device comprising a processor and an associated memory.

17. The method of claim 1 wherein the software-based development tool comprises a simulator control module, a set of interfaces, and circuit element modules each corresponding to an associated one of the integrated circuits.

18. An apparatus for simulating the operation of at least one switch fabric comprising a plurality of integrated circuits, the apparatus comprising:

an information processing device having a processor and a memory;

the information processing device implementing a software-based development tool providing an interface permitting user control of one or more configurable parameters of the switch fabric, the development tool being operative to automatically generate a simulation configuration for the switch fabric based on current values of the configurable parameters;

the simulation configuration being generated without requiring further user input;

the simulation configuration specifying interconnections between the integrated circuits which satisfy the current values of the configurable parameters.

19. An article of manufacture comprising a storage medium containing one or more software programs for use in simulating the operation of at least one switch fabric comprising a plurality of integrated circuits, utilizing a software-based development tool, wherein the one or more software programs when executed implement the steps of:

providing in the software-based development tool an interface permitting user control of one or more configurable parameters of the switch fabric; and

automatically generating a simulation configuration for the switch fabric based on current values of the configurable parameters;

the simulation configuration being generated without requiring further user input;

the simulation configuration specifying interconnections between the integrated circuits which satisfy the current values of the configurable parameters.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None